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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/707,389 | 12/10/2003 | Takayuki Katoh | JP920020250US1 | 1388 |

63203 7590 02/28/2007

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| EXAMINER | |
|---|---|
| YANCHUS III, PAUL B | |
| ART UNIT | PAPER NUMBER |
| 2116 | |

| SHORTENED STATUTORY PERIOD OF RESPONSE | MAIL DATE | DELIVERY MODE |
|---|---|---|
| 3 MONTHS | 02/28/2007 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/707,389 | KATOH ET AL. | |
| | Examiner | Art Unit | |
| | Paul B. Yanchus | 2116 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *21 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-3,5-7 and 9-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-3,5-7 and 15-19* is/are allowed.

6)☒ Claim(s) *9-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

This non-final office action is in response to communications filed on 11/21/06.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 9-11 and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Devlin et al., US Patent no. 6,710,621 [Devlin].

Regarding claim 9, Devlin discloses a power supply controller which controls a power supply unit having a plurality of power supplies each of which can be independently set to a plurality of states, said power supply controller comprising:

a state register circuit to store state values corresponding to a combination of voltages supplied by the power supply unit [inherent that some sort of registers would have to be used by the power controller in the motherboard to store supply voltage data because the data is transferred serially to the motherboard from the daughterboard];

a state value setting combination circuit which generates a change instruction to change the combination of voltages supplied by the power supply unit [daughterboard power requirements circuitry produces one or more control signals, column 10, lines 28-30];

a state value changing combination circuit which changes the state values when the change instruction is received to change the combination of voltages supplied by the power supply unit [power controller on motherboard, column 10, lines 28-39]; and

an output section to transmit the combination of voltages corresponding to the change instruction state values successively changed by the state value changing combination circuit to the power supply unit [connections from Power Controller to Programmable Power supplies in Figure 5].

Because Devlin discloses that the supply voltage data is transferred serially, Devlin also discloses that the changing of the state values is performed one by one in a predetermined order, the order in which the data is transferred to the power control circuitry on the motherboard.

Regarding claims 10 and 11, Devlin discloses an information processor which operates using a plurality of different operating voltages comprising:

a state register section which stores state values corresponding to a combination of voltages supplied to the information processor [inherent that some sort of registers would have to be used by the power controller in the motherboard to store supply voltage data because the data is transferred serially to the motherboard from the daughterboard];

a reference clock oscillator circuit [inherent that some type of clock generator would be used to provide a clock signal to the motherboard or daughterboard circuitry];

a state value setting combination circuit which generates a change instruction to change the combination of voltages supplied to the information processor [daughterboard power requirements circuitry produces one or more control signals, column 10, lines 28-30];

a state value changing combination circuit which changes the state values when the change instruction to change the combination of voltages supplied to the information processor is received [power controller on motherboard, column 10, lines 28-39];

an output section through which the information processor is supplied the combination of voltages corresponding to the state values successively changed by said state value changing combination circuit [connections from Power Controller to Programmable Power supplies in Figure 5]; and

a power supply unit which supplies power to the information processor according to an instruction from said output section [Programmable Power supplies in Figure 5].

Because Devlin discloses that the supply voltage data is transferred serially, Devlin also discloses that the changing of the state values is performed one by one in a predetermined order, the order in which the data is transferred to the power control circuitry on the motherboard.

Regarding claim 14, Devlin discloses information processor which operates using a plurality of power supplies each of which can be independently set in an on or off state, said information processor comprising:

a state register section which stores state values corresponding to a combination of voltages supplied to the information processor [inherent that some sort of registers would have to be used by the power controller in the motherboard to store supply voltage data because the data is transferred serially to the motherboard from the daughterboard];

a reference clock oscillator circuit [inherent that some type of clock generator would be used to provide a clock signal to the motherboard or daughterboard circuitry];

a state value setting combination circuit which generates a change instruction to change the combination of voltages supplied to the information processor [daughterboard power requirements circuitry produces one or more control signals, column 10, lines 28-30];

a state value changing combination circuit which changes the state values when a change instruction to change the combination of voltages supplied to the information processor is received [power controller on motherboard, column 10, lines 28-39];

an output section through which the information processor is supplied the combination of voltages corresponding to the state values successively changed by said state value changing combination circuit [connections from Power Controller to Programmable Power supplies in Figure 5]; and

a power supply unit which supplies power to the information processor according to an instruction from said output section [Programmable Power supplies in Figure 5].

Because Devlin discloses that the supply voltage data is transferred serially, Devlin also discloses that the changing of the state values is performed one by one in a predetermined order, the order in which the data is transferred to the power control circuitry on the motherboard.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Devlin et al., US Patent no. 6,710,621 [Devlin], in view of Reents, US Patent no. 5,860,125.

Regarding claims 12 and 13, Devlin does not disclose enabling the reference oscillator when the change instruction is received and disabling the reference oscillator when the state value combination circuit has stopped supplying the plurality of voltages. However, as shown by Reents, disabling a clock of a circuit when the circuit is not being used is well known in the art as a power saving technique [column 3, lines 57-63]. It would have been obvious to one of ordinary skill in the art to modify the Devlin information processor to use the well known power saving technique of disabling a clock of a circuit when the circuit is not being used to reduce unnecessary power consumption.

### *Allowable Subject Matter*

Claims 1-3, 5-7 and 15-19 are allowed.

### *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul B. Yanchus whose telephone number is (571) 272-3678. The examiner can normally be reached on Mon-Thurs 8:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on (571) 272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Paul Yanchus
February 22, 2007

REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
2/26/07